Digital Circuit Fundamentals 1

FACET®

FESTO

Communication and Radar Technology

Digital and Microprocessor Electronics

Workbook

Festo Didactic
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Workbook

Digital Circuit Fundamentals 1

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Student Workbook

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Introduction

This Student Workbook provides a unit-by-unit outline of the Fault Assisted Circuits for Electronics Training (FACET®) curriculum.

The following information is included together with space to take notes as you move through the curriculum.

- Unit objective
- Fundamentals
- New terms and words for the unit
- Equipment required for the unit
- Exercise objectives
- Exercise discussion
- Exercise notes

The Appendix includes safety information.

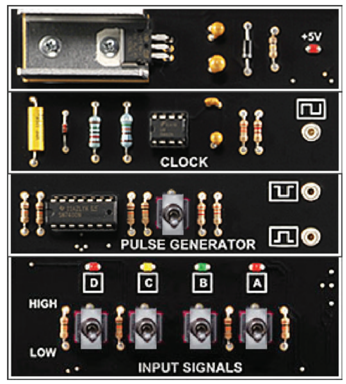
Circuit Board Introduction

UNIT OBJECTIVE

At the completion of this unit, you will be able to identify and operate the circuit blocks on the DIGITAL CIRCUIT FUNDAMENTALS 1 circuit board.

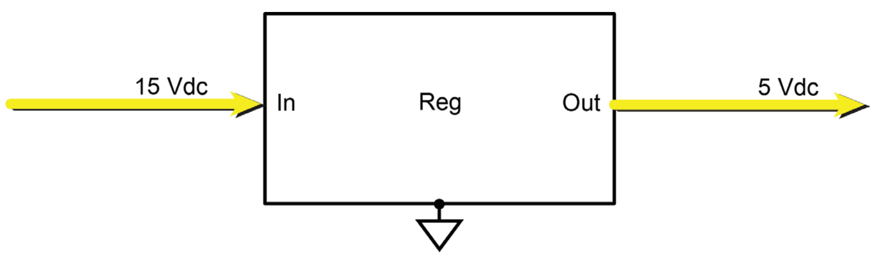
UNIT FUNDAMENTALS

A general purpose circuit block consists of a 5 V regulator, a square wave CLOCK generator, a PULSE GENERATOR circuit, and an INPUT SIGNALS generating set of toggle switches.

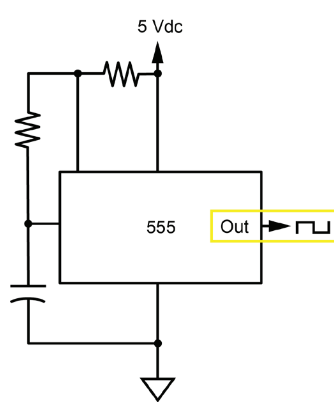


A voltage regulator converts the system's 15 Vdc power supply to 5 Vdc, which is required by the integrated circuits (ICs) on the circuit board.

Power supply voltages are hardwired to all ICs on the circuit board.

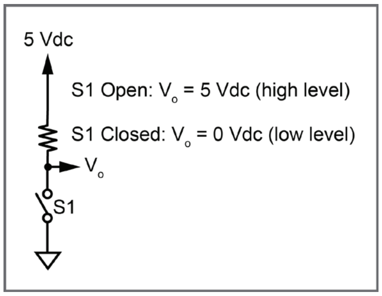


The timer (555 type) CLOCK circuit generates a square wave clock waveform.

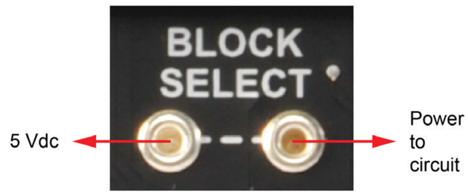


The PULSE GENERATOR toggle switch generates positive- and negative-going signal edges.

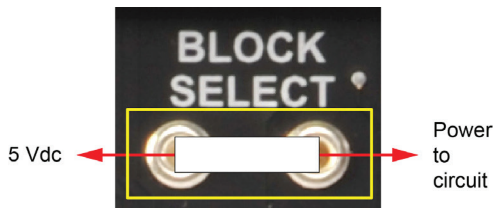
The “at home” position of this toggle switch is in its UP position.
The INPUT SIGNALS toggle switches, labeled A through D, generate high and low TTL digital levels.



The outputs of this section are hardwired to other points on the circuit board that are labeled A through D.
The BLOCK SELECT control powers specified LED circuits.



Two-post connectors and patch leads (interconnecting leads) activate various circuit functions and interconnect circuit blocks.



NEW TERMS AND WORDS

voltage regulator – an IC that maintains a constant output voltage when input voltage or output load changes.

***integrated circuits* (ICs)** – devices that combine the actions of many transistors on one chip.

hardwired – refers to permanent connections made in copper as opposed to connections that must be completed with a wire or test lead.

***timer* (555 type)** – an IC used with external components to generate various waveforms, such as a pulse train.

TTL – transistor-transistor logic.

LED – light-emitting diode; a semiconductor diode that emits light when forward biased.

decoupling capacitors – capacitors that reduce the impedance between the power supply bus and the IC that the bus powers.

pulse train – a free-running and repetitive waveform; usually refers to a square waveform.

gates – the lowest level or functional section of an IC package.

LS – low power Schottky; a logic family that has high speed but low power consumption.

***dual-in-line packages* (DIPs)** – a type of IC package that has the same number of pins on both sides of the device.

EQUIPMENT REQUIRED

FACET® base unit
DIGITAL CIRCUIT FUNDAMENTALS 1 circuit board
Multimeter
Oscilloscope, dual trace
Two-post connectors
Terminal posts

Component Location and Identification

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to locate the major circuit blocks on the circuit board. You will verify your results by correctly identifying circuits and their major components.

DISCUSSION

- The trainer provides circuits which count, add, compare, and shift digital signals. The trainer is organized into five circuit block units. Each unit may use more than one of the ICs as active circuit elements.
- Monolithic ceramic decoupling capacitors prevent instability and are located near their respective devices.
- Circuit blocks are multifunctional. Two-post connectors are used to select and/or connect circuit blocks.
- Test points and LEDs are provided for voltage level verification.
- Titles of each circuit block are indicative of their basic function. The symbols within the IC denote signal function.

Operation of the General Circuits

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to use the general purpose circuits on the circuit boards. You will verify your knowledge by taking voltage and waveform readings.

DISCUSSION

- The four general purpose circuits are the power supply regulator, CLOCK generator, PULSE GENERATOR, and INPUT SIGNALS.
- The power supply regulator uses a 5V voltage regulator to convert 15 Vdc to 5 Vdc. This supply powers all the ICs on the circuit board and the LED groups which have been activated with the BLOCK SELECT function.
- The CLOCK GENERATOR provides timing for several circuits on the circuit board. Using a 555 timer to generate a square wave and various timing components a clock signal of approximately 50 KHz is produced. The 1N4446 signal diode generates a duty cycle waveform of about 50%.
- The PULSE GENERATOR produces complementary pulse output waveforms which are used to ensure a “single-shot” edge (switch debounce) for each switch activation. The PULSE GENERATOR circuits use two 74LS03 gates and a toggle switch.
- INPUT SIGNALS circuit generates four separate TTL voltages labeled D through A. Each signal has two levels: high or low.

IC Package Fundamentals

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to determine IC pin locations for **LS** devices. You will verify your results on the circuit board.

DISCUSSION

- Logic IC devices are available in plastic or ceramic dual in-line package (DIP) packages. The logic devices on the DIGITAL FUNDAMENTALS I circuit board use plastic DIPs.
- The logic devices are not soldered directly to the printed circuit board but are inserted into sockets.
- Pins are counted in a clockwise (CW) direction from a bottom view or counterclockwise (CCW) from a top view (beginning at pin 1).
- Manufacturer's provide specification sheets for their devices. Specific pin terminals and circuit functions are examples of the type of information provided.

NOTES

Asynchronous Ripple Counter

UNIT OBJECTIVE

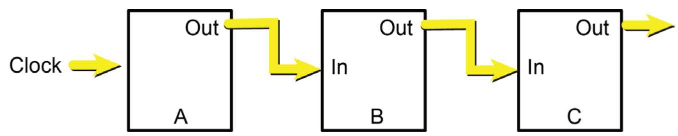
At the completion of this unit, you will have a working knowledge of an asynchronous ripple counter configured from JK flip-flops.

UNIT FUNDAMENTALS

A ripple counter consists of 2 or more flip-flops connected so that the output of each flip-flop is wired to the input of the following flip-flop.

The initial input is called CLOCK.

The output of flip-flop A is connected to the input of flip-flop B. The output of B is connected to the input of C.

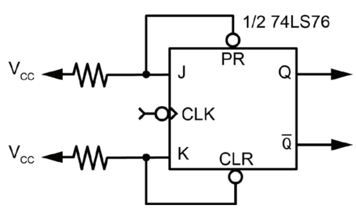


A ripple counter is also called an asynchronous counter because the circuit outputs do not change simultaneously with a common clock.

The asynchronous counter is also referred to as a serial counter.

A JK flip-flop used to construct a ripple counter is configured as a T, or toggle, flip-flop.

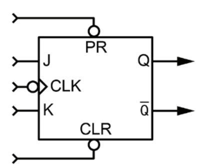
The J and K inputs are pulled to V_{CC}. Q and $\overline{Q}$ are complements; therefore, ripple counters may have complementary outputs. Ripple counters can be set or cleared.



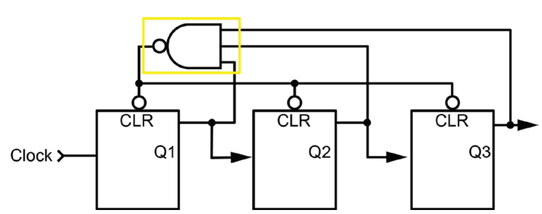
Function Table of JK Flip-Flop LS76A

PR	CLR	J	K	CLK	Q	$\overline{Q}$	
L	X	X	X	X	H	L	(Set flip-flop)
X	L	X	X	X	L	H	(Reset flip-flop)
H	H	H	L	⇩	H	L	(Q high after clock)
H	H	L	H	⇩	L	H	(Q low after clock)
H	H	H	H	⇩	Toggle		

H = High
L = Low
X = Don't care
⇩ = Negative clock edge



The maximum number of counts of a ripple counter may be controlled with feedback. This action, or controlling of the count, is the modulus (sometimes abbreviated MOD) of the counter.



NEW TERMS AND WORDS

ripple counter – an asynchronous or serial counter in which the sections are triggered one at a time, not simultaneously.

asynchronous – a related set of signals that do not change at the same period of time.

T, or toggle, flip-flop – a gate that alters its output state for each clock cycle.

modulus – the number of output states.

nibble – 4 bits of binary data.

word – a group of data bits processed as a single unit. Typically, a word consists of eight bits or two four-bit nibbles.

EQUIPMENT REQUIRED

FACET® base unit
DIGITAL CIRCUIT FUNDAMENTALS 1 circuit board
Multimeter
Oscilloscope, dual trace
Two-post connectors
Terminal posts

Control Functions

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to control the function of an asynchronous ripple counter. You will verify your results by operating a 4-bit ripple counter.

DISCUSSION

- This is a four bit asynchronous ripple counter. The bits are labeled BIT1 through BIT4.
- BIT1 is the least significant bit (LSB). Each input CLOCK cycle produces a change of state, high or low. It takes two CLOCK cycles to generate one output cycle of BIT1. BIT1 divides the CLOCK input by 2.
- BIT2 changes state when clocked by BIT1. It takes four CLOCK cycles to generate one output cycle at BIT2. BIT2 divides the CLOCK input by 4.
- BIT3 divides the CLOCK input by 8. BIT4, the most significant bit (MSB), divides the CLOCK input by 16.
- A nibble is four bits, or half an 8-bit binary word.
- A 4-bit ripple counter generates an output range equivalent to the decimal values 0 through 15.

Waveforms

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to interpret output waveforms of the ripple counter. You will verify your results by observing the waveforms on your oscilloscope.

DISCUSSION

- Two waveforms per stage are generated by the 4-bit ripple counter. There are a total of eight waveforms generated.
- The waveforms generated by the ripple counter verify its asynchronous nature.
- Each output waveform changes its state on the negative edge of the preceding waveform: individual stages are configured from negative edge triggered JK flip-flops.
- Sixteen clock cycles are required to increment the counter through its binary count of 0000 through 1111.
- Relationships between clock frequency, period, and clock division factors illustrate how the ripple counter divides input signals.
- All LEDs appear to be on simultaneously at the 50 kHz clock frequency; therefore, the count sequence will be indistinguishable.

NOTES

Synchronous Counter

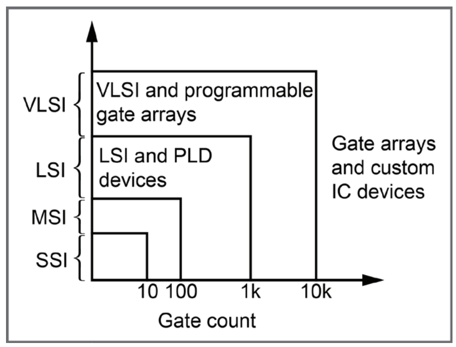
UNIT OBJECTIVE

At the completion of this unit, you will have a working knowledge of an UP/DOWN synchronous counter.

UNIT FUNDAMENTALS

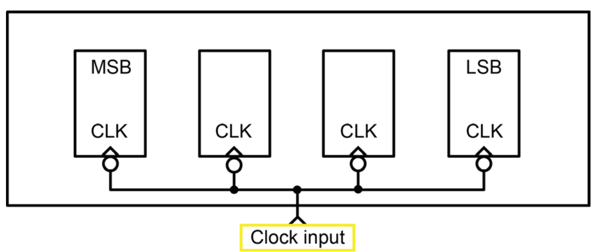
The 74LS193 is a monolithic synchronous reversible (up/down) counter constructed on a single IC substrate.

The IC has a gate complexity of 55 equivalent gates, placing it in the MSI (medium-scale integration) category.

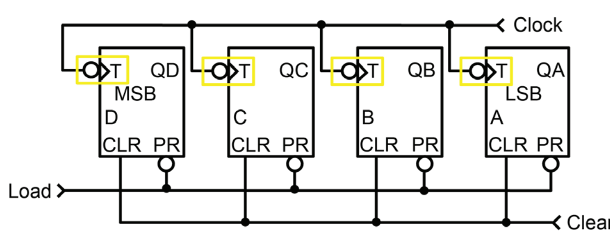


In the LS193 counter, synchronous operation is provided by simultaneous clocking of all flip-flops. This mode of operation ensures that the counter outputs change at the same time.

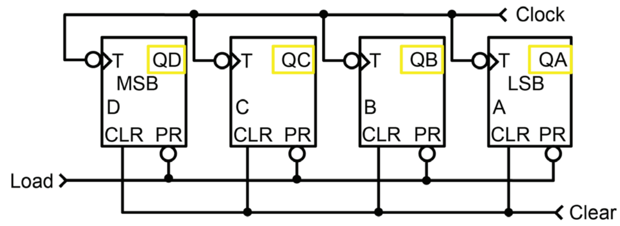
A synchronous counter eliminates the output counting spikes normally associated with asynchronous (ripple-clocked) counters.



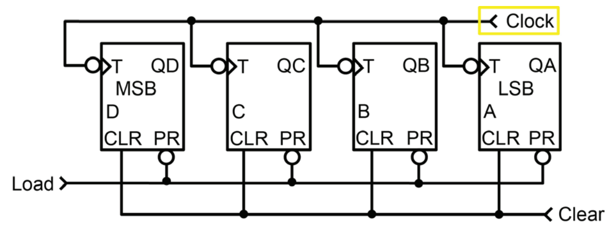
Each section of the LS193 counter is composed of a JK flip-flop configured as a T (toggle) flip-flop.



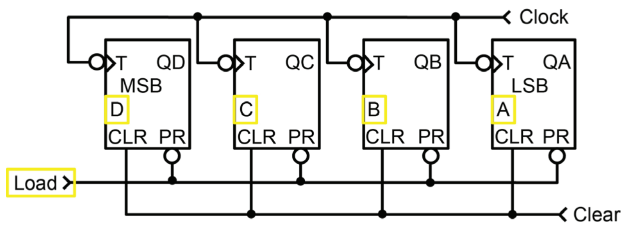
Each counter stage provides a single output (QA through QD).



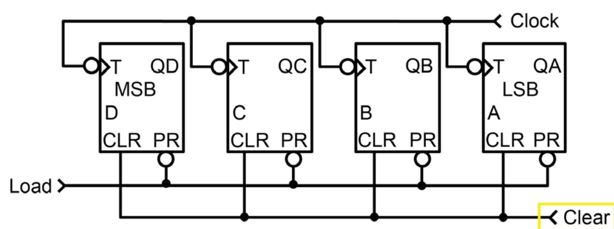
The CLOCK input is common to each stage of the counter and updates all outputs simultaneously.



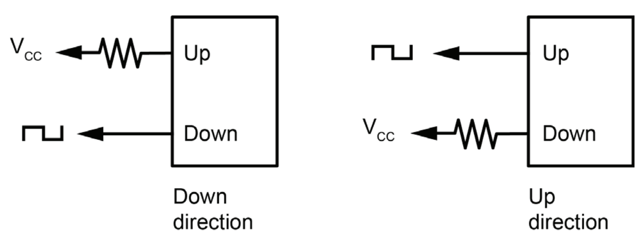
The $\overline{\text{LOAD}}$ input is common to each stage of the counter. LOAD, in conjunction with data inputs A through D, presets each counter stage.



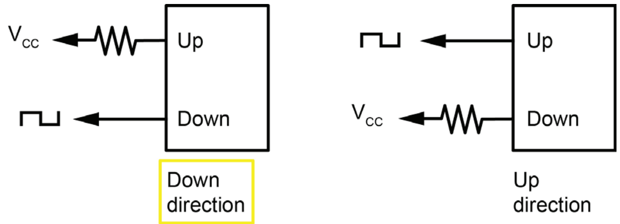
CLEAR is a common input that sets all Q outputs low.



The LS193 counter can count up or down.

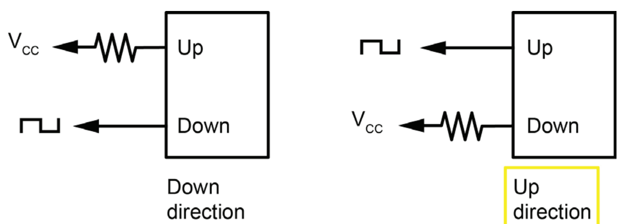


If UP is pulled to V_{CC} and DOWN is pulsed, the count direction is down (HEX B, A, 9, 8, etc.).

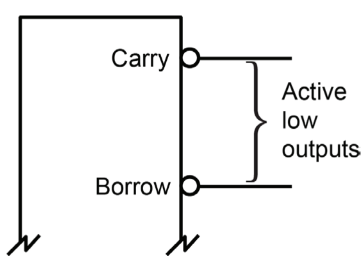


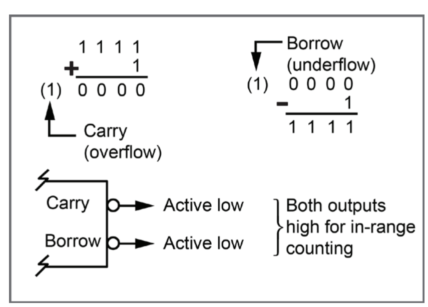
QD	QC	QB	QA	Decimal	HEX
1	1	1	1	15	F
1	1	1	0	14	E
1	1	0	1	13	D
1	1	0	0	12	C
1	0	1	1	11	B
1	0	1	0	10	A
1	0	0	1	9	9
1	0	0	0	8	8
0	1	1	1	7	7
0	1	1	0	6	6
0	1	0	1	5	5
0	1	0	0	4	4
0	0	1	1	3	3
0	0	1	0	2	2
0	0	0	1	1	1
0	0	0	0	0	0

If DOWN is pulled to V_{CC} and UP is pulsed, the count direction is up (HEX 8, 9, A, B, etc.).

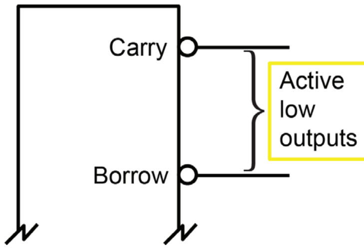


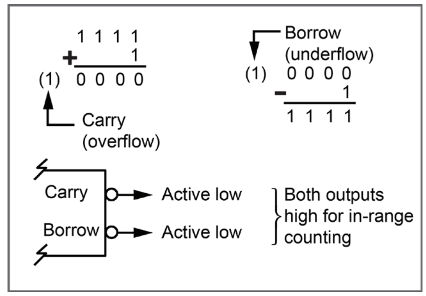
The LS193 counter detects overflow (a count of 15 + 1) and underflow (a count of 0 – 1).



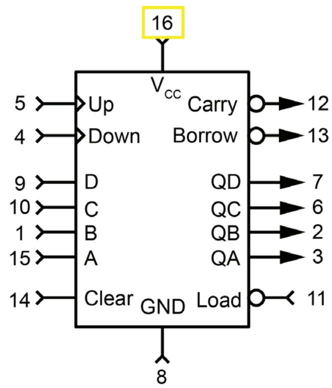


Overflow detection generates an active CARRY output signal. Underflow detection generates an active BORROW output signal.





The pin-out structure of the 74LS193 serial counter indicates a 16-pin device. Your circuit board uses a DIP version.



NEW TERMS AND WORDS

monolithic – a manufacturing process or concept whereby a complete system, like your counter, is fabricated as a single microcircuit.

synchronous – on your counter, it refers to simultaneous output state changes occurring with a common CLOCK input.

overflow – on your UP counter, the condition generated when you increment the 1111 count state.

underflow – on your DOWN counter, the condition generated when you decrement the 0000 counter state.

EQUIPMENT REQUIRED

FACET® base unit
DIGITAL CIRCUIT FUNDAMENTALS 1 circuit board
Multimeter
Oscilloscope, dual trace
Two-post connectors
Terminal posts

Control Functions

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to control the functions of a synchronous counter. You will verify your results by operating a 4-bit counter.

DISCUSSION

- The BLOCK SELECT supplies power to the LEDs. Each LED represents a state of the IC output terminals. LED on = 1 (high state); LED off = 0 (low state)
- The four output bits are labeled QD (MSB) through QA (LSB).
- Inserting a two-post connector and momentarily pulling CLEAR low resets the counter outputs.
- Momentarily pulling LOAD low sets the counter outputs to the same level as the circuit inputs A through D. A through D are controlled by toggle switches which are located on the INPUT SIGNALS circuit.
- A two-post connector must be used to enable the COUNT input function. The connector allows the CLOCK input to be passed to the UP and DOWN inputs of the IC.
- When COUNT and UP are selected the counter increments. When only COUNT is selected the counter decrements.
- Use the STEP input function to override the free-run counting mode and allow single-step clocking. In this operating mode the CLOCK inputs are generated by the toggle switches located in the PULSE GENERATOR circuit.
- Activating the MOD option, with a two-post connector, uses a specific modulus to reset the counter. The MOD circuit point is not an actual modulus feedback signal. It enables a gate to pass the signal to the counter IC CLEAR input.
- The LS193 counter is binary, the 4-bit output represents counts between 0000_2 (\$0) and 1111_2 (\$F), and generates a CARRY and a BORROW.

Waveforms

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to describe the waveforms associated with a synchronous counter. You will verify your results by observing the waveforms on your oscilloscope.

DISCUSSION

- The LS193 synchronous counter has two input signals (UP and DOWN) associated with clocking and count direction.
- All outputs are clocked simultaneously on a synchronous counter.
- The counter has internal gates that allow it to generate CARRY and BORROW output pulses.
- Counter configurations set to increment its value generate a CARRY. Counter configurations set to decrement its value generate a BORROW.
- The pulse width of the CARRY and BORROW outputs equal the pulse width of the UP or DOWN input.

NOTES

4-Bit Shift Register

UNIT OBJECTIVE

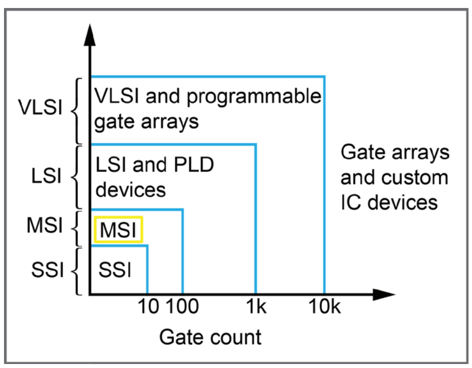
At the completion of this unit, you will have a working knowledge of the 4-BIT SHIFT REGISTER circuit block.

UNIT FUNDAMENTALS

The 74LS194 is a monolithic, bidirectional shift register. The IC has a gate complexity of 46 equivalent gates, placing it in the MSI (medium scale integration) category.

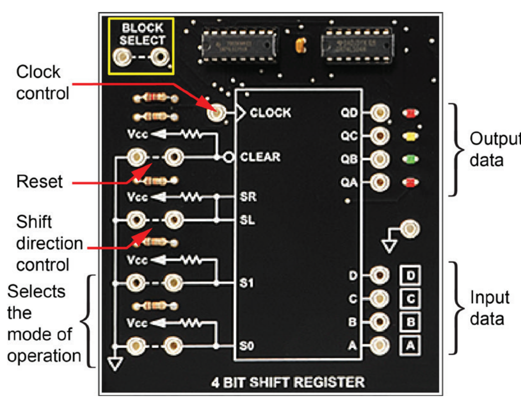
Operation	Function
Parallel load	Preset outputs from inputs
Shift right	Data moves from QA toward QD
Shift left	Data moves from QD toward QA
Inhibit clock	Do nothing

Operational Modes of the LS194

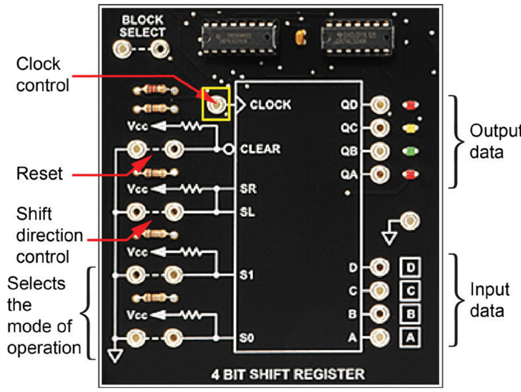


IC features include parallel inputs and outputs, shift right and shift left serial inputs, operating mode control inputs, and a direct overriding CLEAR (reset) input.

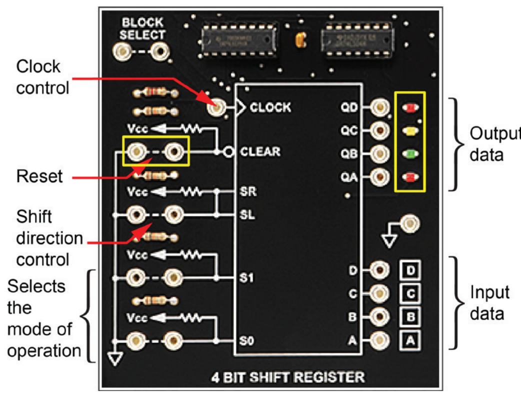
The BLOCK SELECT function, not a part of the IC, controls the application of power to the circuit block LEDs.



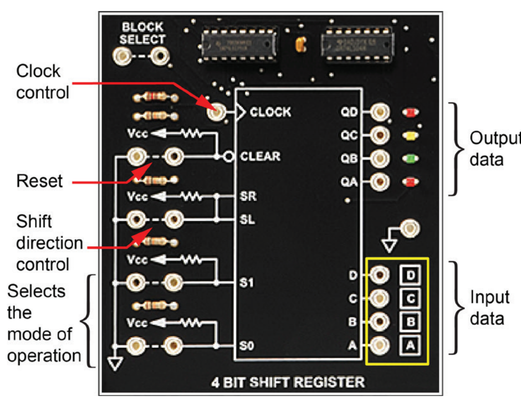
The CLOCK input (positive edge triggered) synchronously shifts data right or left.



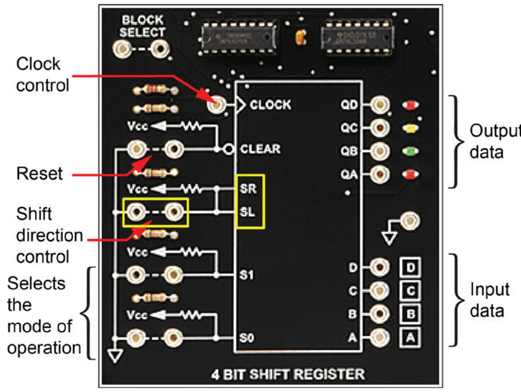
CLEAR, a reset for the shift register, places all outputs (QD through QA) in the LOW, or zero, state (LEDs OFF).



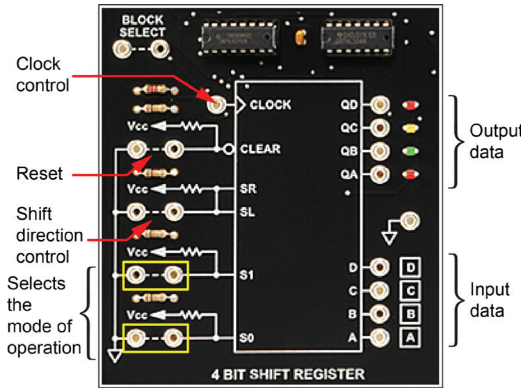
Synchronous parallel loading sets (presets) the register, placing the 4 data bits on the input lines (D through A) at the outputs (QD through QA).



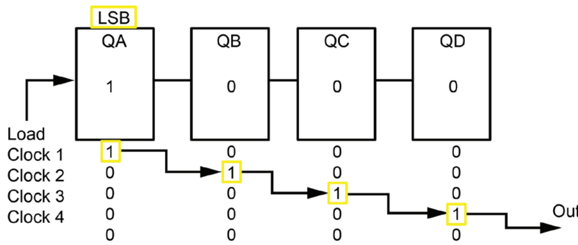
SR (serial right) and SL (serial left) input serial data to the IC.



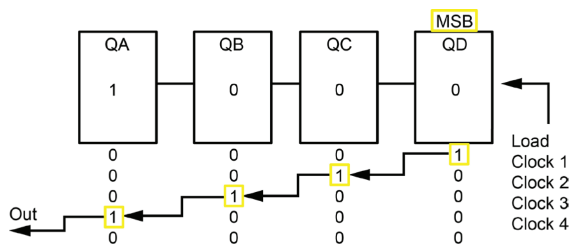
S0 and S1 are the register select inputs: 2 bits control 4 specific functions.



Shift right is defined as a bit or data movement toward QD: a bit of data is shifted from a less significant register toward a more significant register. 0 shifted into a flip-flop resets its output to 0. 1 shifted into a flip-flop sets its output to 1.



Shift left is defined as a bit or data movement toward QA: a bit of data is shifted from a more significant register toward a less significant register. 0 shifted into a flip-flop resets its output to 0. 1 shifted into a flip-flop sets its output to 1.



NEW TERMS AND WORDS

inhibit – to prevent an action such as data shift.

bidirectional – moving in either of two directions (for example, left or right).

shift right – movement of data from a less significant register to a more significant register.

shift left – movement of data from a more significant register to a less significant register.

EQUIPMENT REQUIRED

FACET® base unit
DIGITAL CIRCUIT FUNDAMENTALS 1 circuit board
Multimeter
Oscilloscope, dual trace
Two-post connectors
Terminal posts

Basic Operating Modes

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to select various functions of the shift register. You will verify your results by using the shift register to move data.

DISCUSSION

- Two select lines (S1 and S0) control the operating mode of the shift register.
- When both select lines are high, synchronous parallel loading occurs and the input lines D through A contain data.
- A momentary low on the CLEAR input line clears the shift register.
- Output data refresh and serial data inputs are synchronous with positive transitions of the CLOCK input.
- New serial data enters into the LSB flip-flop when right-shifting data and enters the MSB flip-flop when left-shifting data.

Circuit Waveforms

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to relate the bit movements of a shift register to circuit waveforms. You will verify your results by observing your circuit waveforms on an oscilloscope.

DISCUSSION

- The LS194 is a synchronous shift register. Outputs are updated on the positive transition of the CLOCK waveform.
- CLEAR does not require a CLOCK input; all other operations of the shift register require a minimum of one CLOCK cycle.

NOTES

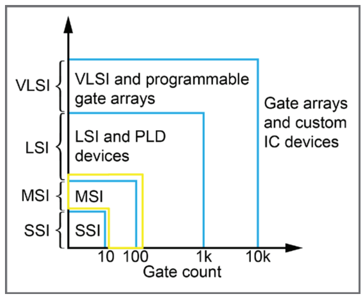
4-Bit Adder

UNIT OBJECTIVE

At the completion of this unit, you will have a working knowledge of a 4-BIT ADDER.

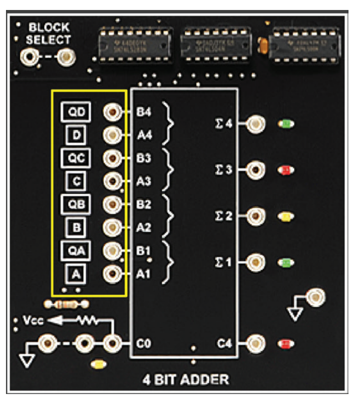
UNIT FUNDAMENTALS

The 74LS283 adder adds two 4-bit binary words. This IC falls into the medium scale integration (MSI) category. The LS283, unlike the LS83 earlier version, has its V_{CC} and GND pins at diagonal corners of the IC, simplifying PCB interconnections.

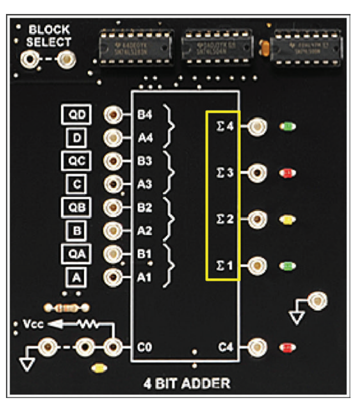


There are 8 input terminals, labeled A through D and QA through QD. A through D comprise one 4-bit word. QA through QD comprise the second 4-bit word.

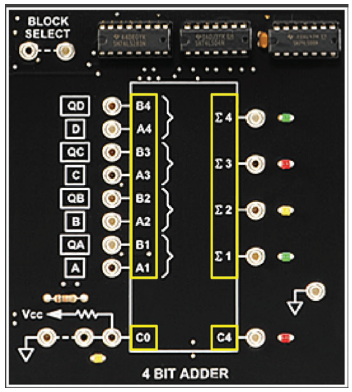
A and QA are the least significant bits (LSB) of the adder. D and QD are the most significant bits (MSB) of the adder.



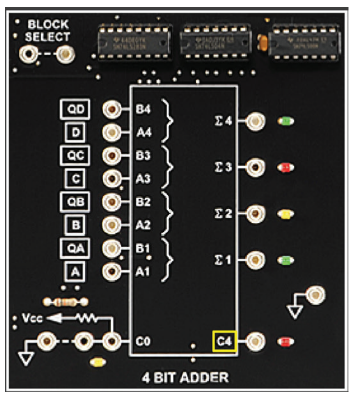
The outputs are referred to as the sum of, which is indicated by the symbol Σ (Σ1 is the sum of A and QA).



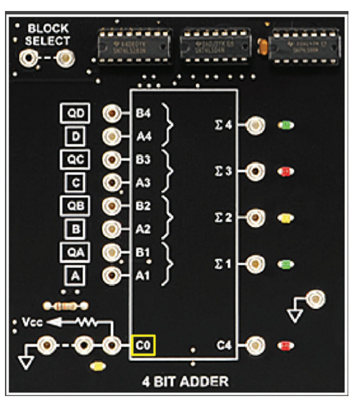
The signal identifiers enclosed within the IC borders are the identifiers assigned by the device manufacturer.



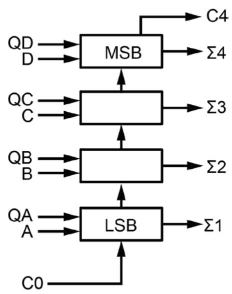
C4 (output of the MSB stage of the counter) indicates an overflow, or a carry. The carry is generated when a binary 1 is added to a binary 1111.

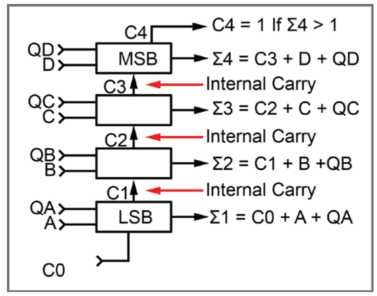


C0 (input to the first, or LSB, stage of the counter) adds 1 to the input side of the adder.



The IC performs binary (or base 2) addition. The base 2 subscript, or radix, indicates a binary weighted number written as $number_2$ (1000_2). Each stage adds its three inputs, generates an output, and internally sends carry information to the next stage in line.





The fundamental rules of binary addition are given below.

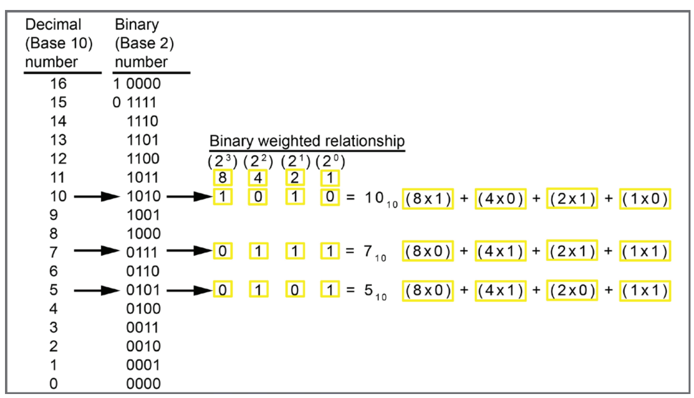
0 + 0 = 0

0 + 1 = 1

1 + 0 = 1

1 + 1 = 0 with a 1 carry or 10_2

EXAMPLE	EXAMPLE WITH A CARRY
0010	0001
+ 0101	+ 0001
0111	0010



NEW TERMS AND WORDS

the sum of – a term indicating that numbers are added to generate a sum.

base 2 – a number expressed in binary form.

radix – a subscript that defines the base of a number.

EQUIPMENT REQUIRED

FACET® base unit
DIGITAL CIRCUIT FUNDAMENTALS 1 circuit board
Multimeter
Oscilloscope, dual trace
Two-post connectors
Terminal posts

Fundamental Binary Addition

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to predict the output of a 4-bit adder. You will verify your results by using a 4-bit adder to add two 4-bit words.

DISCUSSION

- The gates forming the 4-bit adder have additional logic circuit elements which ensure that gates B and C respond to unequal inputs.
- Carry detection is provided by gate A if inputs A and B are both 1.
- Gate B generates a 1 when A = 0 and B = 1. Gate C generates a 1 when A = 1 and B = 0.
- Two cascaded stages have the elements of a two 2-bit word adder.
- The circuit provided with the trainer does not show the internal carry or overflow bits (C1, C2, and C3) but they are included in the overall result.
- Stage A is the LSB stage of the adder. Stage D is the MSB stage of the adder.
- Outputs QD through QA of the SYNCHRONOUS COUNTER circuit block are hardwired as inputs to the 4-bit adder circuit block.
- Inputs D through A of the 4-BIT ADDER circuit block are hardwired to toggle switches D through A of the INPUT SIGNALS circuit.
- Inputs to any one stage are paired: for example A and QA; and C and QC.
- A through D comprise one 4-bit word and QA through QD comprise the second 4-bit word.
- Addition occurs between words only. Addition does not occur within words.

Binary Addition and Carry

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to use input C0 of your adder. You will verify your results by relating circuit waveforms to output binary sum values.

DISCUSSION

- A carry of 1 is activated when the C0 input, to the adder, is pulled to V_{CC}. C0 pulled high adds 1 to the data being summed. C0 pulled to V_{SS} (common or 0V) has no effect on the data being summed.
- An oscilloscope can scan the output waveforms of the adder.
- The overflow output (C4) is active during the complete count 16 interval. This interval equals the time during which the adder output is greater than 15: (C4)0000.

NOTES

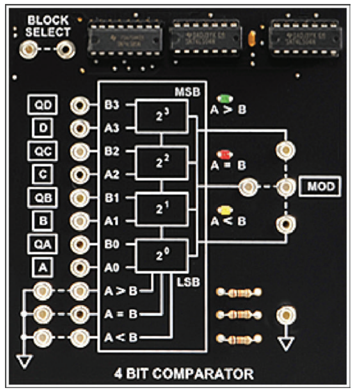
4-Bit Comparator

UNIT OBJECTIVE

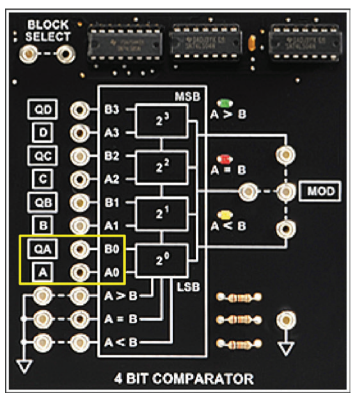
At the completion of this unit, you will have a working knowledge of a 4-bit comparator.

UNIT FUNDAMENTALS

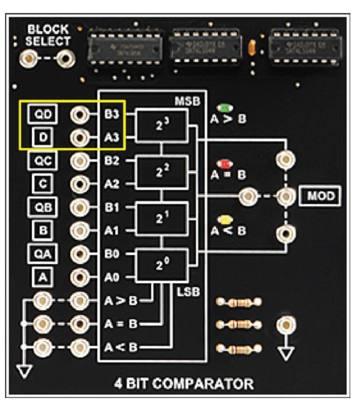
The 74LS85 IC used on your circuit board is a 4-bit magnitude comparator.



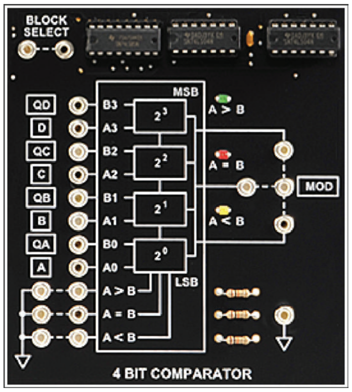
The LSB inputs correspond to the A0 and B0 inputs.

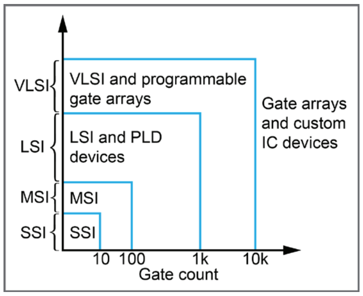


The MSB inputs correspond to the A3 and B3 inputs.

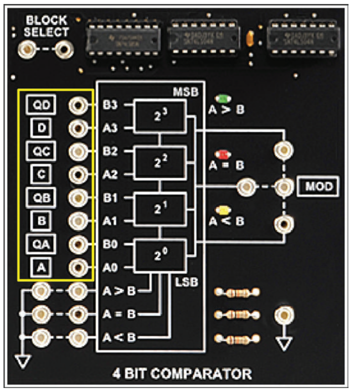


This IC falls into the medium scale integration (MSI) category.

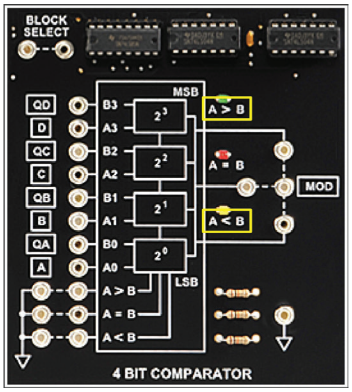




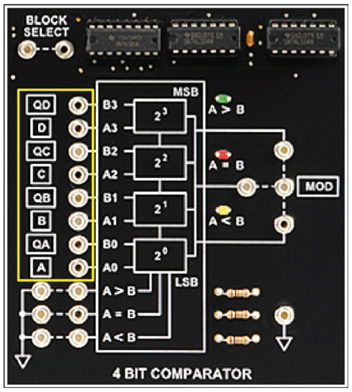
The LS85 comparator makes decisions about two 4-bit words with respect to word A.



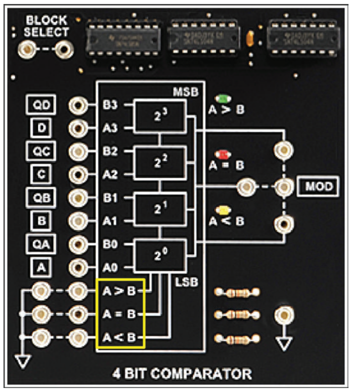
If A is greater than B, then the A > B output is activated. If A is less than B, then the A < B output is activated.



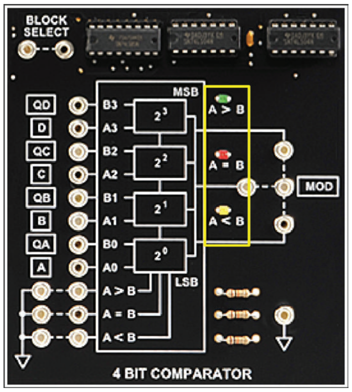
Two 4-bit words comprise the input of the comparator. On the circuit block, word A (A0 through A3) is labeled A through D, and word B (B0 through B3) is labeled QA through QD.



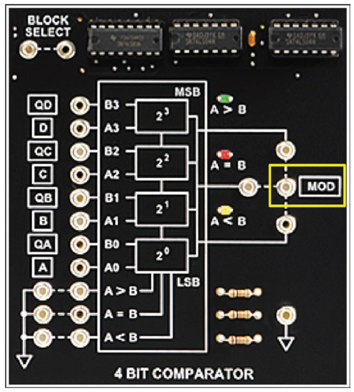
Inputs A > B, A = B, and A < B program the comparator. Programming determines at which state (high or low) the IC A = B output indicates equality.



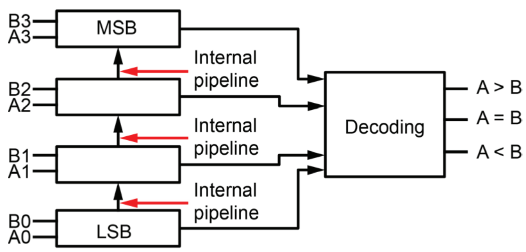
LEDs show the status of each output: on for high and off for low.



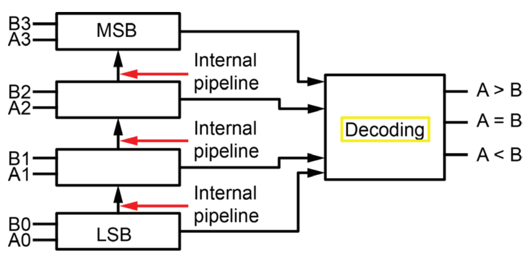
Connections between any one comparator output and the MOD point allow feedback to the SYNCHRONOUS COUNTER circuit block.



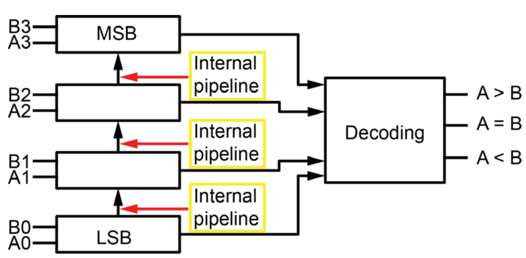
Each stage compares one bit of each word.



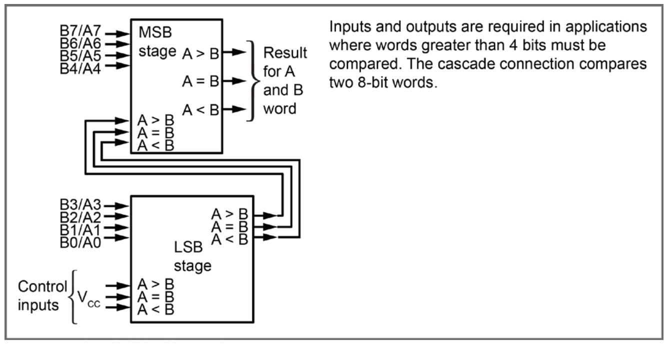
The decision about each comparison is passed to the decoding stage, where all results are combined and placed on the comparator output terminals.



Information between input comparison stages flows through an internal pipeline.

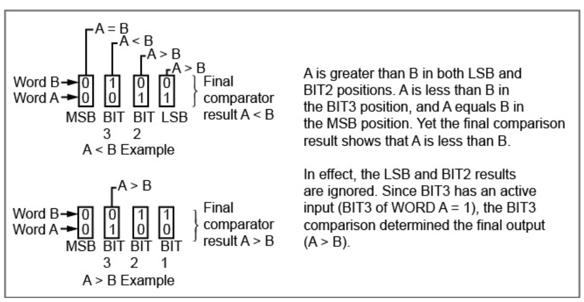


The LS85 comparator has a set of greater than (>), equal to (=), and less than (<) inputs and outputs. The inputs are used to select how a decision is represented at the comparator output.



This table shows comparisons between various 4-bit words.

Word B	1111	1010	0101	0100	0000
Word A	1111	1011	0100	1000	0000
A > B	0	1	0	1	0
A = B	1	0	0	0	1
A < B	0	0	1	0	0



NEW TERMS AND WORDS

magnitude comparator – an IC or circuit used to compare two words and to decide which word has a greater value.

pipeline – refers to a pathway over which data can flow.

EQUIPMENT REQUIRED

- FACET® base unit
- DIGITAL CIRCUIT FUNDAMENTALS 1 circuit board
- Multimeter
- Oscilloscope, dual trace
- Two-post connectors
- Terminal posts

Binary Comparisons

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to perform comparisons of two 4-bit binary words. You will verify your comparisons on the 4-BIT COMPARATOR circuit block.

DISCUSSION

- The four input lines (D through A) on the 4-bit comparator circuit block are controlled by toggle switches D through A on the INPUT SIGNALS circuit block.
- Inputs QD through QA of the 4-BIT COMPARATOR circuit block are hardwired to the SYNCHRONOUS COUNTER circuit block.
- The comparator has three possible outputs (A>B, A<B, and A=B) when two 4-bit words are compared.
- The two basic operating modes of this comparator are: words A and B are equal and words A and B are not equal. There are three input control lines which determine the output code for each mode of the comparator.
- Truth tables provide the operating states and control codes for equal inputs and for not equal inputs.

Modulus Control

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to set the modulus of a counter with a comparator. You will verify your results by using a comparator to drive the CLEAR input of a synchronous counter.

DISCUSSION

- The LS85 comparator outputs generate time slots that reflect the relationship between two 4-bit words.
- When a comparator output signal is wired to the CLEAR input of a counter, the signal can be used to reset the counter once a predetermined binary value has been reached.
- Controlling the binary value of word A while word B cycles between binary values generates comparator outputs which are active for a specific period of time. By selecting the appropriate output the comparator can control the modulus of the counter.

NOTES

Appendix A – Safety

Safety is everyone's responsibility. All must cooperate to create the safest possible working environment. Students must be reminded of the potential for harm, given common sense safety rules, and instructed to follow the electrical safety rules.

Any environment can be hazardous when it is unfamiliar. The FACET® computer-based laboratory may be a new environment to some students. Instruct students in the proper use of the FACET® equipment and explain what behavior is expected of them in this laboratory. It is up to the instructor to provide the necessary introduction to the learning environment and the equipment. This task will prevent injury to both student and equipment.

The voltage and current used in the FACET® Computer-Based Laboratory are, in themselves, harmless to the normal, healthy person. However, an electrical shock coming as a surprise will be uncomfortable and may cause a reaction that could create injury. The students should be made aware of the following electrical safety rules.

1. Turn off the power before working on a circuit.
2. Always confirm that the circuit is wired correctly before turning on the power. If required, have your instructor check your circuit wiring.
3. Perform the experiments as you are instructed: do not deviate from the documentation.
4. Never touch "live" wires with your bare hands or with tools.
5. Always hold test leads by their insulated areas.
6. Be aware that some components can become very hot during operation. (However, this is not a normal condition for your FACET® course equipment.) Always allow time for the components to cool before proceeding to touch or remove them from the circuit.
7. Do not work without supervision. Be sure someone is nearby to shut off the power and provide first aid in case of an accident.
8. Remove power cords by the plug, not by pulling on the cord. Check for cracked or broken insulation on the cord.

We Value Your Opinion!

We invite readers of this manual to send us their tips, feedback and suggestions for improving the book. Please send these to did@de.festo.com.